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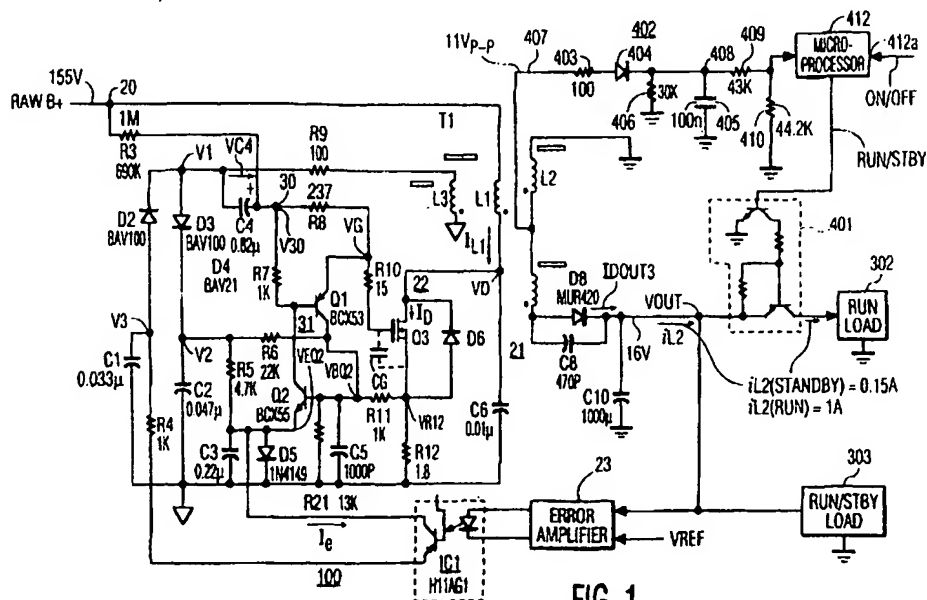
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(54) **Power supply with synchronized power on transition**

(57) A power supply operates in a run mode of operation and in a standby, burst mode of operation. When, for example, a user initiates a power-on request command, an on/off control signal is applied to an input terminal of a microprocessor. The microprocessor mon-

itors an end time of a dead time interval of a burst mode cycle and generates a synchronized control signal for turning on a switch. The switch turns on immediately after the end of the dead time interval. The turned on switch couples a run mode load to a filter capacitor of the power supply.



**FIG. 1**

## Description

[0001] The invention relates to a power supply having a burst mode operation and a run mode operation.

## Background

[0002] A typical switch mode power supply (SMPS) includes a switching transistor coupled to a primary winding of power transferring transformer for periodically applying an input supply voltage to the primary winding. It is known to operate the SMPS in a run mode of operation and in a standby mode of operation. During a run mode operation, pulses of current are developed in a secondary winding of the transformer at a high frequency and are rectified for periodically replenishing a charge in a filter or smoothing capacitor. An output supply voltage, developed in the capacitor, is connected to energize a load.

[0003] In the run mode of operation, the SMPS operates in a continuous mode. In the standby mode of operation, it may be desirable to operate the SMPS in a burst mode for reducing power dissipation. In a given cycle of the burst mode, the high frequency current pulses are developed in the transformer windings. The current pulses are followed by a relatively long interval, referred to herein as dead time interval, of several milliseconds, in which no current pulse is produced.

[0004] An on/off control signal may be generated in a microprocessor. The microprocessor is referenced to a potential referred to as cold ground that is conductively isolated from a mains supply voltage. Whereas, a control circuit of the SMPS may include a portion that is conductively non-isolated from the mains supply voltage. The transformer forms a conductive isolation barrier.

[0005] It may be desirable to avoid the need for using an additional isolation barrier to apply on/off control information from the conductively isolated microprocessor to the non-isolated SMPS control circuit for changing between the continuous and burst modes.

[0006] An advantageous type of a SMPS is a zero voltage switching SMPS. In zero voltage switching SMPS, switching on the transistor occurs when the voltage between the main current conducting terminals of the transistor is zero for minimizing switching losses. It may be desirable to operate the zero voltage switching SMPS in the burst mode, during standby.

[0007] In a zero voltage switching SMPS, embodying an inventive feature, the standby mode is initiated by disconnecting a run mode load from the filter capacitor via a switch. Thereby, the run mode load ceases consuming load current. Because the run mode load circuit is de-energized, a feedback loop of the SMPS causes the transistor to conduct in a substantially shorter duty cycle than in the run mode. The short duty cycle in successive switching cycles of the transistor causes the zero voltage switching SMPS to operate in a standby, burst mode.

[0008] A transition from the burst mode to the run mode operation is initiated by coupling the run mode load to the filter capacitor via the switch. The increased load current is sensed and results in an increased duty cycle in the transistor. The increased duty cycle causes the zero voltage switching SMPS to operate in the continuous, run mode. Thus, advantageously, the need for using an additional isolation barrier for changing between the continuous and burst modes is avoided.

[0009] The filter capacitor voltage may be used for energizing the microprocessor, during the standby mode. It may be desirable to prevent a significant decrease in the capacitor voltage, during a transition interval from the burst mode to the run mode operation. Preventing the discharge of the filter capacitor avoids a possible malfunction. For example, the microprocessor might, disadvantageously, cease operation if its supply voltage were to decrease excessively.

[0010] A user may issue a power-on command via, for example, a remote control arrangement. If the switch that couples the run load to the capacitor were to be turned on, during the dead time interval, the capacitor voltage could, undesirably, excessively decrease. This is so because current pulses are not produced.

[0011] In carrying out an inventive feature, in response to a user issued power on command, the microprocessor generates a synchronized on/off control signal for turning on the switch. The switch is turned on immediately after the end of the dead time interval for coupling the run mode load to the filter capacitor in synchronization with the end of the dead time interval.

[0012] During the dead time interval, when current pulses are not produced, the run mode load is de-coupled from the filter capacitor. Therefore, advantageously, the filter capacitor is not excessively discharged. The result is that, advantageously, the supply voltage does not decrease, during the dead time interval. Furthermore, each current pulse that occurs immediately after the dead time interval replenishes the charge in the filter capacitor.

[0013] Assume, for example, that the increase in load current is not sufficient to disable the burst mode operation in a first attempt. The microprocessor will, advantageously, cause the switch to be turned off for the duration of the following dead time interval. As a result, discharging the filter capacitor is, advantageously, prevented. At the end of the dead time interval that follows the first attempt, the microprocessor will cause the switch to be turned on in a second attempt. At that time, the load current may be sufficiently high so that the burst mode operation ceases and the continuous run mode begins.

## Summary

[0014] A switch mode power supply, embodying an inventive feature includes an output stage for generating output supply pulses in a run mode of operation and in

a first portion of a burst mode cycle, during standby mode of operation. The output supply pulses are disabled, during a second portion of the burst mode cycle. A control signal indicative of the occurrence of one of the first and second portions of the burst mode cycle and an on/off signal are generated. A switch responsive to the on/off signal and to the control signal and coupled to the output stage selectively energizes a run mode load circuit at a predetermined time in a burst mode cycle, during a transition between the standby and the run modes of operation.

#### Brief Description of the Drawings

##### [0015]

FIGURE 1 illustrates a power supply, embodying an inventive feature, operating in a burst mode, during standby;

FIGURES 2a, 2b and 2c illustrate waveforms useful for explaining the operation of the circuit of FIGURE 1, in the run mode;

FIGURES 3a and 3b illustrate waveforms useful for explaining the operation of the circuit of FIGURE 1, in the standby, burst mode; and

FIGURES 4a, 4b, 4c and 4d illustrate waveforms useful for explaining the operation of the circuit of FIGURE 1 in a transition from the burst mode to the run mode.

#### Description of the Preferred Embodiment

[0016] FIGURE 1 illustrates a tuned SMPS 100, embodying an aspect of the invention. In FIGURE 1, an N-type, metal oxide semiconductor (MOS) power transistor Q3 operating as a transistor switch has a drain electrode coupled through a primary winding L1 of a transformer T1 to a terminal 20 of an input supply, direct current (DC) voltage RAW B+. Transformer T1 serves as an isolation transformer for providing hot ground-cold ground isolation barrier. Voltage RAW B + is derived from, for example, a filter capacitor coupled to a bridge rectifier that rectifies a mains supply voltage, not shown.

[0017] A source electrode of transistor Q3 is coupled to a non-isolated, hot ground I via a current sensor or sampling resistor R12. A damper diode D6 operating as a switch is coupled in parallel with transistor Q3 and is included in the same package with transistor Q3 to form a bi-directional switch 22. Capacitor C6 is coupled in parallel with diode D6 and in series with winding L1 to form with an inductance of winding L1 a resonant circuit 21 when switch 22 is non conductive.

[0018] A secondary winding L2 of transformer T1 is coupled to an anode of a peak rectifying diode D8 and to an isolated or cold ground for generating an output voltage VOUT in a filter capacitor C10 that is coupled to a cathode of diode D8. Voltage VOUT is coupled to a run load circuit 302, during a run mode of operation, via

a series coupled run load switch 401. Switch 401 is controlled by a control signal RUN/STBY, embodying an inventive feature, produced by a microprocessor 412 for maintaining switch 401 turned on, during the run mode.

[0019] An error amplifier 23 is responsive to voltage VOUT and to a reference voltage VREF. A photo-coupler IC1 includes a light emitting diode. An emitter electrode of the transistor of photo-coupler IC1 is coupled to a negative DC voltage V3 via a resistor R4. A collector electrode of the transistor of photo-coupler IC1 is coupled to capacitor C3. Opto-coupler IC1 serves for isolation. An error collector current Ie of the opto-coupler IC1 is indicative of an amount by which voltage VOUT is greater than reference voltage VREF and, thus, of the difference between them.

[0020] A comparator transistor Q2 has a base electrode that is coupled via a resistor R11 to a junction terminal between the source electrode of transistor Q3 and current sensor resistor R12. Transistor Q2 compares a base voltage VBQ2 of transistor Q2 to an error voltage VEQ2 developed at the emitter of transistor Q2. Voltage VBQ2 includes a first portion that is proportional to a source-drain current ID in transistor Q3. A DC voltage V2 is coupled via a resistor R6 to the base of transistor Q2 to develop a second portion of voltage VBQ2 across resistor R11.

[0021] DC voltage V2 is also coupled via a resistor R5 to a feedback loop filter formed by capacitor C3 to form a current source that charges capacitor C3. Error current Ie is coupled to capacitor C3 for discharging capacitor C3. A diode D5 is coupled between the emitter of transistor Q2 and ground. Diode D5 limits voltage VEQ2 to diode D5 forward voltage and limits the maximum current in transistor Q3.

[0022] The collector electrode of transistor Q2 is coupled to the base electrode of a transistor Q1 and the collector electrode of transistor Q1 is coupled to the base electrode of a transistor Q2 to form a regenerative switch 31. A control voltage VG of transistor Q3 is developed at the emitter of transistor Q1 that forms an output terminal of regenerative switch 31 and is coupled to the gate electrode of transistor Q3 via a resistor R10.

[0023] A secondary winding L3 of transformer T1 is coupled via a resistor R9 for producing an alternating current (AC) voltage V1. Voltage V1 is AC-coupled via a capacitor C4 and a resistor R8 to the emitter of transistor Q1 to generate drive voltage VG of transistor Q3. AC-coupled voltage V1 is coupled via a collector resistor R7 to the collector electrode of transistor Q2 and to the base electrode of transistor Q1. Voltage V1 is also rectified by a diode D2 to generate voltage V3 and by a diode D3 to generate voltage V2.

[0024] A resistor R3 coupled between the source of voltage RAW B+ and a terminal 30 of capacitor C4 that is remote from winding L3 charges capacitor C4 when voltage RAW B + is turned on. When voltage VG on the gate electrode of transistor Q3 exceeds a threshold voltage of MOS transistor Q3, transistor Q3 conducts, caus-

ing a drain voltage VD of transistor Q3 to decrease. As a result, voltage V1 becomes positive and reinforces voltage VG for maintaining transistor Q3, in a positive feedback manner, fully turned on.

[0025] FIGURES 2a-2c illustrate waveforms useful for explaining the operation of tuned SMPS 100 of FIGURE 1. Similar symbols and numerals in FIGURES 1 and 2a-2c indicate similar items or functions.

[0026] During an interval t0-t10 of a given period T of FIGURE 2c, current ID of conductive transistor Q3 of FIGURE 1 is up-ramping. Consequently, a corresponding non-resonant current pulse portion of a current IL1 in winding L1 is up-ramping and stores magnetic energy in the inductance associated with winding L1 of transformer T1. At time t10 of FIGURE 2c, voltage VBQ2 of FIGURE 1, containing an up-ramping portion derived from the voltage across resistor R12, exceeds a triggering level of regenerative switch 31 that is determined by voltage VEQ2 and turns on transistor Q2. Current flows in the base of transistor Q1. Therefore, regenerative switch 31 applies a low impedance at the gate electrode of transistor Q3. Consequently, gate electrode voltage VG of FIGURE 2a is reduced to near zero volts and turns off transistor Q3 of FIGURE 1. When transistor Q3 is turned off, drain voltage VD of FIGURE 2b increases and causes voltage V1 of FIGURE 1 that is coupled from winding L3 to decrease. The charge stored in gate-source capacitance CG maintains latch mode operation until time t20 of FIGURE 2a.

[0027] When voltage VG becomes smaller than required to maintain sufficient collector current in transistor Q1 of FIGURE 1, a forward conduction on the base electrode of transistor Q2 ceases and, consequently, latch operation mode in regenerative switch 31 is disabled. Afterwards, voltage V1 that continues to decrease causes a negative portion 40 of voltage VG of FIGURE 2a to maintain transistor Q3 of FIGURE 1 turned off.

[0028] When transistor Q3 is turned off, drain voltage VD increases as shown during interval t10-t20 of FIGURE 2b. Capacitor C6 of FIGURE 1 limits the rate of increase of voltage VD such that transistor Q3 is completely non conductive before voltage VD increases appreciably above zero voltage. Thereby, switching losses and radiated switching noise are, advantageously, reduced. Resonant circuit 21 that includes capacitor C6 and winding L1 oscillates, during interval t10-t30 of FIGURE 2b, when transistor Q3 of FIGURE 1 is turned off. Capacitor C6 limits the peak level of voltage VD. Therefore, advantageously, no snubber diode and resistor are needed so that efficiency is improved and switching noise is reduced.

[0029] The decrease in voltage VD prior to time t30 of FIGURE 2b, causes voltage V1 of FIGURE 1 to become a positive voltage. At time t30 of FIGURE 2b, voltage VD is close to zero volts and slightly negative, causing damper diode D6 of FIGURE 1 to turn on and to clamp voltage VD of FIGURE 2b to approximately zero volts. Thus, resonant circuit 21 of FIGURE 1 exhibits a half

cycle of oscillation. After time t30 of FIGURE 2b, voltage VG of FIGURE 2a becomes increasingly more positive, because of the aforementioned change in polarity of voltage V1 of FIGURE 1.

[0030] The following turn on of transistor Q3 is delayed by a delay time that is determined by the time constant of resistor R8 and gate capacitance CG until after time t30 of FIGURE 2b when voltage VD is nearly zero volts. Therefore, minimal turn-on losses are incurred and switching noise is reduced.

[0031] Negative feedback regulation of voltage VOUT is achieved by varying voltage VEQ2 in filter capacitor C3. When Voltage VOUT is larger than voltage VREF, current Ie discharges capacitor C3 and decreases voltage VEQ2. Therefore, the threshold level of comparator transistor Q2 is decreased. Consequently, the peak value of current ID in transistor Q3 and the power delivered to the load circuit, not shown, are reduced. On the other hand, when voltage VOUT is smaller than voltage VREF, current Ie is zero and the current in resistor R5 increases voltage VEQ2. Consequently, the peak value of current ID in transistor Q3 and the power delivered to the load circuit, not shown, are increased. Thus, the control circuit of transistor Q3 that includes regenerative switch 31 provides duty cycle modulation of current ID in transistor Q3, in accordance with voltage VEQ2.

[0032] Tuned SMPS 100 operates in a current mode control, on a current-pulse by current-pulse control basis. The current pulse of current ID during interval t0-t10 of FIGURE 2c, flowing in transistor Q3 of FIGURE 1, terminates at time t10 of FIGURE 2c when it reaches the threshold level of transistor Q2 of FIGURE 1 that is determined by voltage VEQ2 and is established by error current Ie forming an error signal. The error signal actually controls the peak current of the current pulse of current ID that flows in the inductance of winding L1. The control circuit corrects instantaneously in a feed forward manner for input voltage variations of voltage B+ without using the dynamic range of error amplifier 23. In this way, both the advantages of current mode regulation and of tuned SMPS are obtained.

[0033] FIGURES 3a and 3b illustrate waveforms of a voltage V30 of FIGURE 1 at terminal 30 useful for explaining the operation in a standby, burst mode of SMPS 100. When transistor Q3 is turned on, voltage V30 is approximately equal to gate voltage VG that controls transistor Q3. The waveform of voltage V30 of FIGURE 3b includes a time expanded active interval tA and tB, when switching operations occur in transistor Q3 of FIGURE 1, during a burst mode period tA-tC of FIGURE 3a. During a relatively long dead time interval tB-tC, no switching cycles occur in transistor Q3 of FIGURE 1. Similar symbols and numerals in FIGURES 1, 2a, 2b, 2c, 3a and 3b indicate similar items or functions.

[0034] During a dead time interval that ends at time tA of FIGURE 3b, capacitor C4 of FIGURE 1 is charged in a ramping manner via resistor R3 at a rate determined by the R3, C4 time constant for developing a positive

voltage VC4. At time tA, positive voltage V30 reaches a threshold level of transistor Q3 of FIGURE 1. Consequently, high frequency switching cycles are produced in transistor Q3. During interval tA-tB, a positive peak voltage V30PEAK of voltage V30 of FIGURE 3b exceeds the threshold level of transistor Q3 of FIGURE 1. Therefore, the high frequency switching cycles continue in transistor Q3. In each switching cycle of transistor Q3, transistor Q1 is turned on, as explained before. Therefore, capacitor C4 is slightly discharged. The discharging current in transistor Q1 exceeds the charging current in resistor R3. Therefore, voltage VC4 is down-ramping. Voltage VC4 level shifts voltage V1 in a direction that tends to decrease positive peak voltage V30PEAK of FIGURE 3b. At time tAB, positive peak voltage V30PEAK decreases to a value that is smaller than the threshold level of transistor Q3 of FIGURE 1. Switching operation in transistor Q3 cease at time tB, and the next dead time interval. tB-tC follows. From time tB to time tC of FIGURE 3a, capacitor C4 is charged via resistor R3, as explained before.

**[0035]** When, for example, a user initiates a power-off request command via, for example, a remote control arrangement, not shown, a control signal ON/OFF is applied to an input terminal 412a of microprocessor 412. Microprocessor 412 of FIGURE 1 generates control signal RUN/STBY at a LOW state for turning off run load switch 401. Turned off switch 401 de-couples run mode load circuit 302 of FIGURE 1 from filter capacitor C10 for initiating and maintaining standby, burst mode of operation. Thereby, load circuit 302 is de-energized and a load current iL2 in load circuit 302 ceases. On the other hand, load circuit 303 coupled to capacitor C10 includes stages that are energized, during the standby mode.

**[0036]** Capacitor C10 charging current IDOUT3 is small, when load circuit 302 is de-coupled. Because capacitor C10 charging current IDOUT3 of FIGURE 1 is small when load circuit 302 is de-energized, the feedback loop causes transistor Q3 to conduct in a substantially shorter duty cycle than in the run mode. The short duty cycle in successive switching cycles of transistor Q3 produce standby, burst mode operation of SMPS 100.

**[0037]** Advantageously, SMPS 100 includes both the zero voltage switching feature, in the run mode, as explained before, and the burst mode feature, in the standby mode. Both features take advantage of the self oscillation feature of SMPS 100.

**[0038]** The values of resistor R3 and capacitor C4 are selected in accordance with the required length of dead time interval tB-tC. The value of resistor R8 is selected for insuring operation in the burst mode. If the value of resistor R8 were too large, the discharging current in transistor Q1 will be too small and the positive peak voltage V30PEAK of voltage V30 of FIGURE 3b will not decrease below the threshold level of transistor Q3 of FIGURE 1. Advantageously, by selecting sufficiently small value of resistor R8, burst mode operation is assured

when short duty cycle occur in successive switching cycles of transistor Q3.

**[0039]** FIGURES 4a, 4b and 4c illustrate waveforms useful for explaining a transition from the standby mode to the run mode in SMPS 100 of FIGURE 1. Similar symbols and numerals in FIGURES 1, 2a, 2b, 2c, 3a, 3b, 4a, 4b and 4c indicate similar items or functions. During a burst portion t1-t2 of FIGURE 4c of a given burst mode cycle t1-t3, pulses 407 developed in winding L2 of FIGURE 1 are rectified in an envelope detector 402 for developing an envelope detected pulse signal 408 in capacitor 405 of FIGURE 1. Envelope detector 402 includes a resistor 403 coupled between a portion of winding L2 of transformer T1 and an anode of a rectifying diode 404. A cathode of diode 404 is coupled to a filter capacitor 405, coupled in parallel with a resistor 406. Pulses developed in winding L2 are rectified in diode 404 for developing envelope detected signal 408 in capacitor 405. Signal 408 is coupled via a voltage divider that includes a resistor 409 and a resistor 410 to microprocessor 412.

**[0040]** FIGURE 4c illustrates the waveform of signal 408, during the standby mode and during a transition to the run mode. The transition to the run mode begins at time t3. Pulse signal 408 forms a logical level HIGH, outside a dead time interval t2-t3. During dead time interval t2-t3, burst mode pulses 407 of FIGURE 1 are absent and signal 408 of FIGURE 4c is at a logical LOW level.

**[0041]** When, for example, a user initiates a power-on request command via, for example, a remote control arrangement, not shown, control signal ON/OFF at the appropriate state is applied to input terminal 412a of microprocessor 412. Control signal ON/OFF of FIGURE 4b may occur at a non-synchronized time with respect to signal 408 of FIGURE 4c, for example, at time t8 of FIGURE 4b, during dead time interval t2-t3. As a result, microprocessor 412 of FIGURE 1 begins searching for an occurrence at time t3 of FIGURE 4c of a LOW-to-HIGH transition 408U of envelope detected signal 408. Immediately after time t3 of FIGURE 4c, microprocessor 412 of FIGURE 1 generates synchronized control signal RUN/STBY at the HIGH state for turning on switch 401. It should be understood that the generation of synchronized control signal RUN/STBY can be alternatively accomplished using dedicated logic circuit responsive to envelope detected signal 408 and control signal ON/OFF. Such hardware solution can be used instead of generating signal RUN/STBY under program control in microprocessor 412.

**[0042]** In carrying out an inventive feature, switch 401 is turned on for coupling run mode load circuit 302 of FIGURE 1 to filter capacitor C10 immediately after end time t3 of dead time interval t2-t3 of FIGURE 4c. During a dead time interval portion t8-t3, when current pulses IDOUT3 of FIGURE 1 are not produced, run mode load circuit 302 cannot discharge capacitor C10. Therefore, advantageously, output supply voltage VOUT of FIGURE 1 does not decrease, during interval t8-t3 of FIG-

URE 4a. In contrast, had switch 401 of FIGURE 1 been turned on, during interval t8-t3 of FIGURE 4b, voltage VOUT of FIGURE 4a would have decreased significantly, as shown by a broken line 222 in FIGURE 4a because of the absence of current pulses IDOUT3 of FIGURE 1. Each current pulse IDOUT3 that occurs immediately after dead time interval t2-t3 of FIGURES 4a-4c replenishes filter capacitor C10 of FIGURE 1. Thereby, advantageously, power supply start-up is facilitated.

[0043] Assume, for example, that a magnitude of load current iL2 in the burst mode portion at time t4 of FIGURE 4c is insufficient to disable the burst mode operation after LOW-to-HIGH transition 408U of envelope detected signal 408 occurs. Consequently, a LOW-to-HIGH transition 408D of envelope detected signal 408 occurs and another burst mode cycle will follow.

[0044] In carrying out a further inventive feature, microprocessor 412 will, advantageously, cause switch 401 to be turned off for the duration of a following dead time interval, not shown, that follows time t4 of FIGURE 4c. As a result, discharging filter capacitor C10 of FIGURE 1 is, advantageously, prevented. At the end of the dead time interval, not shown, that follows time t4 of FIGURE 4c, when a following LOW-to-HIGH transition 408U, not shown, of envelope detected signal 408 occurs, the magnitude of load current iL2 of FIGURE 1 may be sufficient to disable the burst mode operation. Consequently, SMPS 100 will continue operating in the continuous run mode. Thereby, advantageously, a second start-up attempt would be facilitated.

#### Claims

1. A switch mode power supply, comprising:

an output stage for generating output supply pulses in a run mode of operation and in a first portion of a burst mode cycle, during standby mode of operation, said output supply pulses being disabled, during a second portion of said burst mode cycle;

means for generating a control signal indicative of the occurrence of one of said first and second portions of said burst mode cycle;

a source of an on/off signal; and  
a switch responsive to said on/off signal and to said control signal and coupled to said output stage for selectively energizing a run mode load circuit at a predetermined time in a burst mode cycle, during a transition between said standby and said run modes of operation.

2. A power supply according to Claim 1, wherein said switch couples said output stage to said run mode load circuit, throughout operation in said run mode of operation.

3. A power supply according to Claim 1 wherein said output stage is responsive to a first signal indicative of a magnitude of said output supply pulses for generating said output supply pulses between corresponding dead time intervals in said burst mode, when said magnitude is within a range of values and for generating said output supply pulses without said dead time intervals in said run mode of operation, when said magnitude is outside said range of values.

4. A power supply according to Claim 1 wherein said switch energizes said run mode circuit in synchronization with said control signal, during said transition.

5. A power supply according to Claim 1 wherein said control signal generating means comprises an envelope detector.

6. A power supply according to Claim 1 further comprising, a filter capacitor, wherein said output stage generates current pulses in said filter capacitor for developing a filtered, output supply voltage and wherein said switch couples said filter capacitor to said run mode load circuit in said run mode and decouples said capacitor from said run mode load circuit in said standby, burst mode.

7. A power supply according to Claim 1, wherein said switch de-couples said run mode load circuit from said output stage, during said second portion, as long as said output supply pulses are disabled, and couples said run mode load circuit to said output stage, when the generation of said output supply pulses begins.

8. A power supply according to Claim 1, wherein said output stage is coupled to a standby mode load circuit for energizing said standby mode load circuit, during said standby mode of operation.

9. A power supply according to Claim 1 further comprising, a microprocessor responsive to said on/off signal and to said control signal for generating a switch control signal that is coupled to a control terminal of said switch.

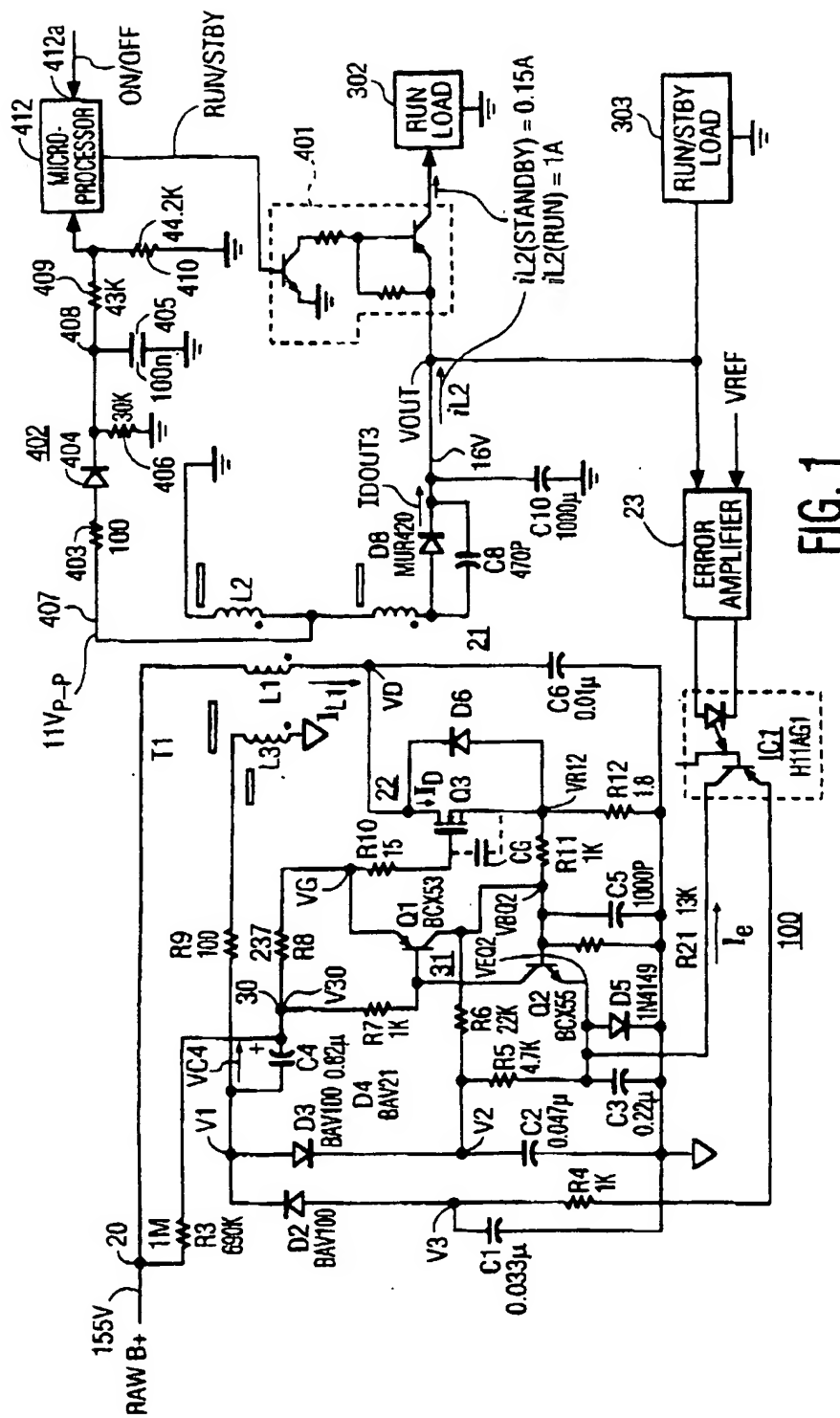


FIG. 1

